# ROCgdb, GDB and AMDGPU debugging

**Lancelot SIX**

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# Agenda

- AMDGPU architecture overview and programming model.
- ROCgdb.
- State of AMDGPU support in upstream GDB.



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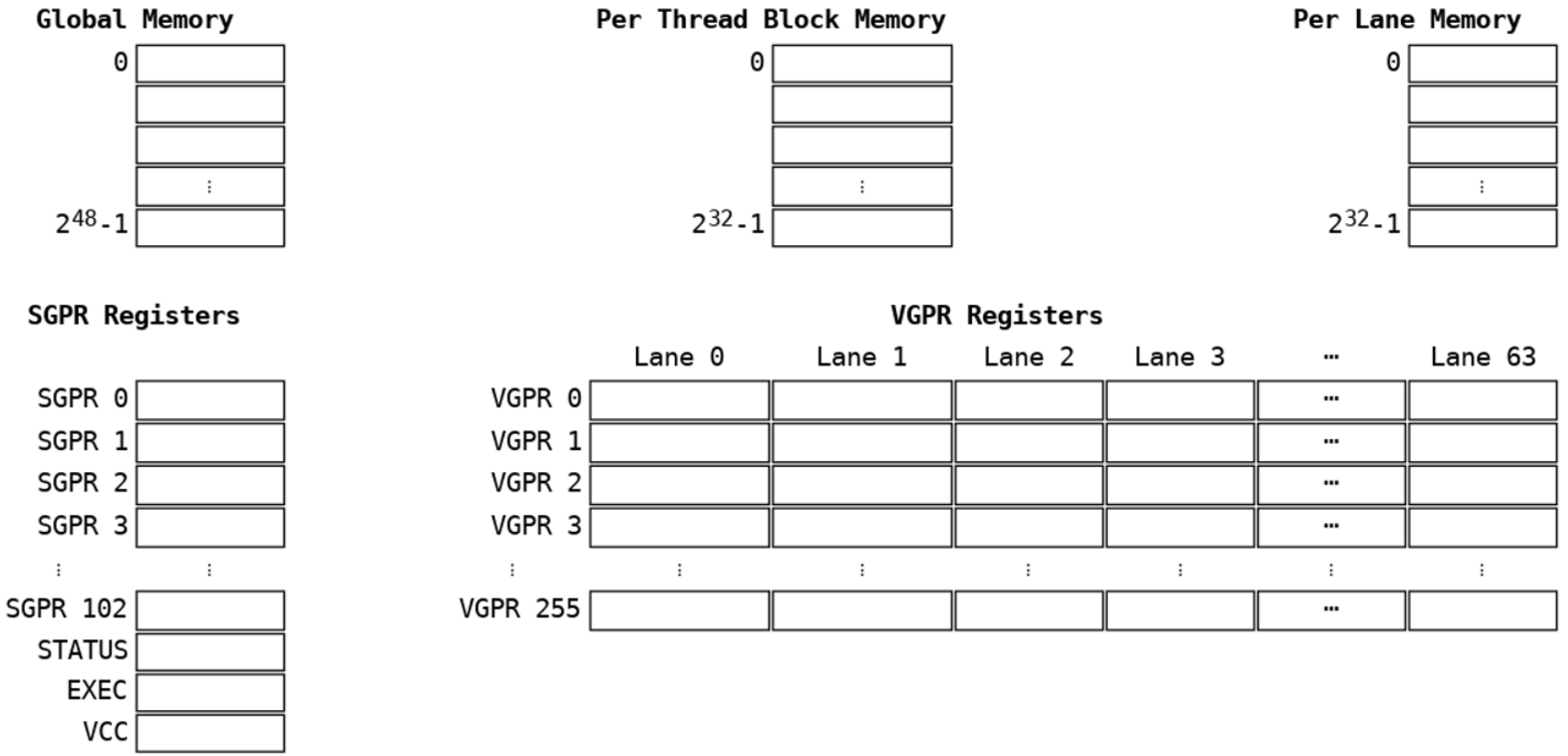
# Abstract AMDGPU architecture




- Multiple processing elements form a compute unit.
- Multiple compute units form a GPU.



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# The HIP "hello world"

```
#include <hip/hip_runtime.h>

__global__ void
kern (int *arr) {
  arr[blockIdx.x * blockDim.x + threadIdx.x] += 2;
}


int
main () {
  const size_t block_size = 64, blocks = 16,
               size = block_size * blocks;
  std::array<int, size> data = {};


  int *device_ptr;
  hipMalloc (&device_ptr, size * sizeof (int));
  hipMemcpyHtoD (device_ptr, data.data (), size * sizeof (int));

  kern<<<blocks, block_size>>> (device_ptr);


  hipMemcpyDtoH (data.data (), device_ptr, size * sizeof (int));
  return EXIT_SUCCESS;
}
```

GPU/device code

CPU/host code



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# Host threads and GPU threads (waves) under single inferior

- Waves are mapped to threads in GDB.
- Same program with unified memory.

```
(gdb) info threads
  Id   Target Id                                         Frame
  1    Thread 0x7ffff7e69a80 (LWP 152926) "a.out" 0x…f41 in ?? () from …/libhsa-runtime64.so.1
  2    Thread 0x7fffeb3ff640 (LWP 152929) "a.out" __GI___ioctl (fd=3, request=3222817548) …
  5    Thread 0x7ffff62d7640 (LWP 152933) "a.out" __GI___ioctl (fd=3, request=3222817548) …
* 6    AMDGPU Wave 1:1:1:1 (0,0,0)/0 "a.out"      kern (arr=0x7fffe9c00000) at simple.cpp:5
  7    AMDGPU Wave 1:1:1:2 (0,0,0)/1 "a.out"      kern (arr=0x7fffe9c00000) at simple.cpp:5
  8    AMDGPU Wave 1:1:1:3 (1,0,0)/0 "a.out"      kern (arr=0x7fffe9c00000) at simple.cpp:5
  …
```



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# GPU Threads (waves)'s Target Id

```
(gdb) info threads
…
                   /- agent
                   | /- queue
                   | | /- dispatch
                   | | | /- wave id
                   | | | |
  6    AMDGPU Wave 1:1:1:1 (0,0,0)/0 "a.out"      kern (arr=0x7fffe9c00000) at simple.cpp:5
                             ^^^^^  |
                                |    \- wave number in work group
                                \- work group coordinates in work grid
…
```

- "info {agent, queue, dispatch}" commands also available.



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# Lanes

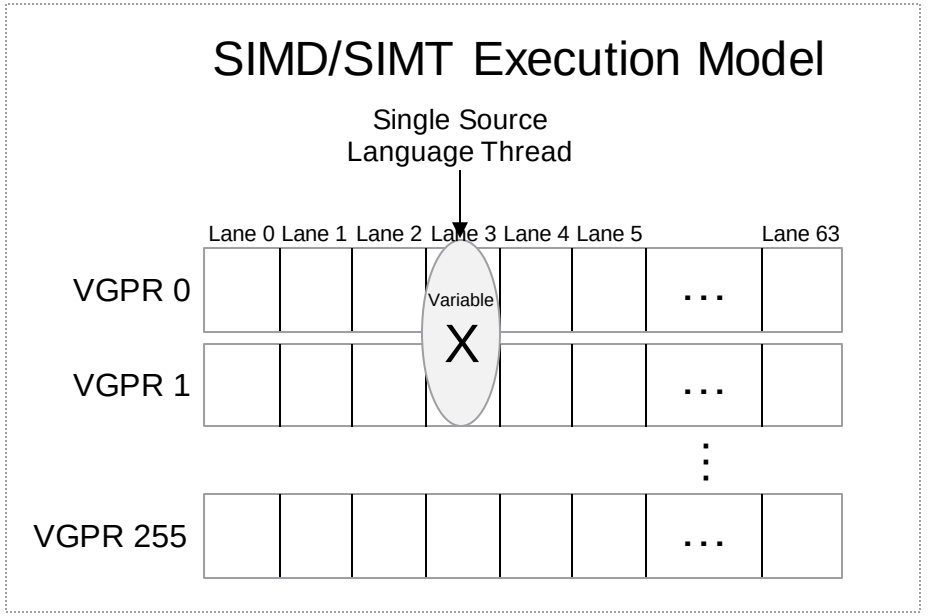
New entity under threads: threads become vectorized, multiple lanes under one thread.

GDB threads are mapped to GPU waves. All lanes progress side-by-side forming a wavefront.

One physical PC for the whole thread (for all lanes), but:

- Each lane works with its own slice of the register set, on its share of data, its version of locals in scope.
- Lanes can be seen as multiple "regular" threads running in lockstep.

"current lane" concept added (augmenting "current inferior", "current thread").



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# Lanes commands

```
(gdb) info lanes
  Id   State Target Id                                    Frame
* 0    A     AMDGPU Lane 1:1:1:1/0 (0,0,0)[0,0,0]   kern (arr=0x7fffe9c00000) …
  1    A     AMDGPU Lane 1:1:1:1/1 (0,0,0)[1,0,0]   kern (arr=0x7fffe9c00000) …
  2    A     AMDGPU Lane 1:1:1:1/2 (0,0,0)[2,0,0]   kern (arr=0x7fffe9c00000) …
  3    A     AMDGPU Lane 1:1:1:1/3 (0,0,0)[3,0,0]   kern (arr=0x7fffe9c00000) …
  4    A     AMDGPU Lane 1:1:1:1/4 (0,0,0)[4,0,0]   kern (arr=0x7fffe9c00000) …
  5    A     AMDGPU Lane 1:1:1:1/5 (0,0,0)[5,0,0]   kern (arr=0x7fffe9c00000) …
  6    A     AMDGPU Lane 1:1:1:1/6 (0,0,0)[6,0,0]   kern (arr=0x7fffe9c00000) …
…
  31   A     AMDGPU Lane 1:1:1:1/31 (0,0,0)[31,0,0] kern (arr=0x7fffe9c00000) …
(gdb) lane 8
[Switching to thread 6, lane 8 (AMDGPU Lane 1:1:1:1/8 (0,0,0)[8,0,0])]
#0  kern (arr=0x7fffe9c00000) at simple.cpp:5
5         arr[blockIdx.x * blockDim.x + threadIdx.x) += 2;
```



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# SIMT Lanes's Target Id

```
                  /- agent
                  | /- queue
                  | | /- dispatch
                  | | | /- wave id
                  | | | |
                  | | | |
AMDGPU Lane 1:1:1:1/8 (0,0,0)[8,0,0]   kern (arr=0x7fffe9c00000) at simple.cpp:5
                        |  ^^^^^  ^^^^^
                        |    |      |
                        |    |      \- work item coordinates in work group
                        |    \- work group coordinates in work grid
                        \- lane index
```



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# SIMT and Lane divergence


```
if (foo (lid)) {
  elem = in[lid] + 1;
} else {
  elem = in[lid] + 3;
}
```

Else lanes

Then lanes


```
// if (foo (lid)) {
     NoOp;
// } else {
     elem = in[lid] + 3;
// }
```


```
// if (foo (lid)) {
     elem = in[lid] + 1;
// } else {
     NoOp;
// }
```



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# Without lane divergence support, step 1

**Stepping stops in all branches => surprising**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

>> (1)    if (tid % 2)                    <<<<<<<<<
   (3)      elem = in[tid] + 1;
          else
   (2)      elem = in[tid] + 3;
   (4)    atomicAdd (out, elem);
        }
```



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# Without lane divergence support, step 2

**Stepping stops in all branches => surprising**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

   (1)    if (tid % 2)
   (3)      elem = in[tid] + 1;
          else
>> (2)      elem = in[tid] + 3;        <<<<<<<<<
   (4)    atomicAdd (out, elem);
        }
```



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# Without lane divergence support, step 3

**Stepping stops in all branches => surprising**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

   (1)    if (tid % 2)
>> (3)      elem = in[tid] + 1;        <<<<<<<<<
          else
   (2)      elem = in[tid] + 3;
   (4)    atomicAdd (out, elem);
        }
```



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# Without lane divergence support, step 4

**Stepping stops in all branches => surprising**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

   (1)    if (tid % 2)
   (3)      elem = in[tid] + 1;
          else
   (2)      elem = in[tid] + 3;
>> (4)    atomicAdd (out, elem);       <<<<<<<<<
        }
```



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# With lane divergence support, step 1

**Stepping doesn't stop if current lane is inactive => intuitive**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

>> (1)    if (tid % 2)                    <<<<<<<<<
   (X)      elem = in[tid] + 1;
          else
   (2)      elem = in[tid] + 3;
   (3)    atomicAdd (out, elem);
        }
```



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# With lane divergence support, step 2

**Stepping doesn't stop if current lane is inactive => intuitive**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

   (1)    if (tid % 2)
   (X)      elem = in[tid] + 1;
          else
>> (2)      elem = in[tid] + 3;          <<<<<<<<<
   (3)    atomicAdd (out, elem);
        }
```



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# With lane divergence support, step 3

**Stepping doesn't stop if current lane is inactive => intuitive**

```
        __device__ void
        function (unsigned tid, const int *in, int *out)
        {
          int elem;

   (1)    if (tid % 2)
   (X)      elem = in[tid] + 1;
          else
   (2)      elem = in[tid] + 3;
>> (3)    atomicAdd (out, elem);       <<<<<<<<<
        }
```



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# Multiple address spaces support

- Introducing the `address_space#offset` notation.
- Architecture address-spaces are not a source language concept!
- Use "`maintenance print address-spaces` " to list the address-spaces supported by the current target.

```
__device__ int some_global = 8;
__shared__ int some_shared;

__device__ int
func (int *arr)
{
  int some_private = 8;
  return some_shared + some_private;
}
```

```
(gdb) p &some_global
$1 = (int *) 0x7ffff617d1a8 <some_global>
(gdb) p &some_shared
$2 = (int *) local#0x0
(gdb) p &some_private
$3 = (int *) private_lane#0x40
(gdb) x private_lane#0x40
private_lane#0x40:      0x00000008
(gdb) p *(int*)private_lane#0x40
$4 = 8
```



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# Useful things to know

- Exceptions are reported for the entire wave.

- Memory exceptions are not precise by default.
  - If available, use "`set amdgpu precise-memory on`" to identify the faulty instruction (impacts performances).

- On some architectures, attaching to a process shows:

```
AMDGPU Wave 1:3:?:1 (?,?,?)/? "attached_process" …
```

  - Use "HSA_ENABLE_DEBUG=1" before starting the process.

- On some architectures, at most one process can be debugged at a time.



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# DWARF and GPU architectures

- Challenges with current DWARF standard:
  - AMD GPUs have multiple address spaces, a "numerical address" is not sufficient to locate an object in memory.
  - The stack is not implemented in the default address space.
  - Support for divergent control flow of SIMT hardware.
  - And more…
- DWARF extensions to overcome those issues implemented in downstream LLVM + ROCgdb:
  - https://llvm.org/docs/AMDGPUDwarfExtensionsForHeterogeneousDebugging.html
- "DWARF for GPU" workgroup involving multiple vendors working to propose changes to the DWARF committee:
  - https://dwarfstd.org/issues/230524.1.html
  - More to come…



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# AMDGPU support status in upstream GDB

| Feature | Status |
|---|---|
| ~~Driver support in upstream Linux kernel~~ | ✓ |
| ~~Wave control (breakpoint, single-step, interrupt & resume)~~ | ✓ |
| ~~Disassembly~~ | ✓ |
| ~~Precise memory operations~~ | ✓ |
| Displaced stepping | Pending |
| Stack unwinding | Blocked by DWARF |
| Printing variables | Blocked by DWARF |
| Address spaces support | Blocked by DWARF |
| Lane debugging | Need to agree with other vendors on the UI.<br>Need DWARF to write testcases. |
| Watchpoints | Need DWARF to write testcases |



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# Additional resources

- ROCgdb:
  - https://github.com/ROCm/ROCgdb/
  - https://rocm.docs.amd.com/projects/ROCgdb/en/latest/ROCgdb/gdb/doc/gdb/Heterogeneous-Debugging.html
  - https://rocm.docs.amd.com/projects/ROCgdb/en/latest/ROCgdb/gdb/doc/gdb/AMD-GPU.html
- Rocm-dbgapi (used by GDB to control AMDGPU devices):
  - https://github.com/ROCm/ROCdbgapi/
- "Anatomy of ROCgdb" at GNU Cauldron 2022:
  - https://gcc.gnu.org/wiki/cauldron2022#cauldron2022talks.anatomy_of_rocgdb_gdb_for_amd_gpus
  - https://www.youtube.com/watch?v=X1iZ_Ta7jOo
- "DWARF extensions for optimized SIMT/SIMD (GPU) debugging" at Linux Plumbers Conference 2021:
  - https://lpc.events/event/11/contributions/1012/
  - https://www.youtube.com/watch?v=Iv2WO67nklc



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